REMARKS

The original filing of the present application included Claims 1-9. No additions of claims have been made in the prosecution of the present application. Claims 1-7 are currently pending in the present application with claims 1 and 7 being amended and claims 8 and 9 being cancelled. Claims 1-9 stand rejected in the Office Action dated march 26, 2003 and this amendment addresses the rejections made in this Office Action. The Amendment filed on June 17, 2003 in response to the Final Amendment was not entered.

Rejection of Claims 1-6 under 35 U.S.C. § 102(b)

Claims 1-6 stand rejected under 35 U.S.C. §102(b) as being anticipated by Shinya, U.S. Patent No. 5,170,158.

The present claimed invention is an arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device. The arrangement includes a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal. A control bus is coupled to the common terminal for communicating corresponding signals to the plurality of switches. A plurality of local buses are separated from one another for communicating corresponding signals. Each of the plurality of local buses have a first bus section coupled to the second terminal of respective ones of the plurality of semiconductor switches. Each first bus section extends in a manner so as to cross the control bus. Each of the plurality of local buses have a second bus section connected to the first bus section and have conductors thereof coupled in a local, clustering bus arrangement to the second terminals of the respective ones of the plurality of switches. The associated switches have the third terminals thereof coupled to the consecutively disposed column conductors of the array of the display device.

The local clustering bus arrangement connecting the local buses to the second terminals of the plurality of switches is disclosed in the specification and shown clearly in Figure 3. With respect to claim 1 and as can be seen from this figure and its accompanying description, the clustering bus arrangement groups brightness information carrying conductors into local "clusters", each cluster forming a local bus. The brightness information carrying conductors are coupled to four switches having gate electrodes that share, in common a conductor. The first terminal of each group of switches are coupled to the control bus.

The present claimed invention decreases the number of times the local buses cross over the control bus. The disadvantages associated with crossing of the control bus are described with reference to Figure 2 of the inventive disclosure, specifically on page 6 lines 10-14, addressing the fact that

> "the number of capacitive crossovers increases geometrically with the number of data-word conductors DW(i) according to the equation: number of crossovers = number of brightness information carrying conductors DB(j) x 1/2 x (number of data-word conductors DW(i))."

The present claimed invention reduces the number of times conductors DWC(i) cross the bus of conductors DW(i) in order to reduce dynamic power dissipation and improve yield by coupling the plurality of local buses to the second terminal of the plurality of switches in a clustering bus arrangement. The inventive application discusses its achievement of the stated objective with reference to Figure 3 stating on page 6, lines 17-29, summarizing on lines 24-29:

> "In this example, the number of crossovers of brightness information carrying conductors DB (j)-to-data-word conductors DW (i) have been reduced by a factor of about 4:1. This, advantageously, reduces dynamic power

dissipation, improves yield and reduces the crosstalk among the brightness information carrying-conductors."

On page 7, lines 18-20, the interconnections of the prior art diagram shown in Figure 2 and the inventive diagram on Figure 3 are compared as 28,800 crossovers are present in the prior art and only 7,450 total crossovers are present in the present claimed invention.

Furthermore, the claimed plurality of local buses which are separated from one another in the local clustering bus arrangement reduces the capacitance formed between the local buses. As is claimed in claim 1 and can be seen in Figure 3, each local bus is associated with a respective group of switches whereby a given one of said plurality of local buses having a first bus section coupled to said second terminal of respective ones of said plurality of semiconductor switches.

Shinya discloses a display device having a driver circuit for driving data lines in a matrix display panel according to input digital signals. The driver circuit includes a number of digital-to-analog (D/A) converters, which number is less than the number of pixels contained in one horizontal scanning line. The D/A converters are repeatedly used to sequentially convert portions of the input digital image signal corresponding to one horizontal scanning line. The analog signals obtained by each D/A conversion are retained by a sample-and-hold circuit. When storage for one horizontal scanning line is completed, the signals are simultaneously delivered to the data lines.

Shinya neither discloses nor suggests "a plurality of local buses that are separated from one another...having a first bus section...each said first bus section extending in a manner to cross said control bus" as in the present claimed invention. Shinya discloses a plurality of individual conductors, each conductor extending from the output of a respective DAC 15. Each of the conductors is then connected to a plurality of switches in a manner similar to the prior art disclosed in the specification and shown in Figure 2 of the

present specification. Shinya neither discloses nor suggests a plurality of local buses that are separated from one another. Only a plurality of individual conductors all crossing over one another is shown and described with the control line crossing each conductor numerous times. As discussed above, this configuration is contrary to the purpose of the present claimed invention. In this embodiment, each individual conductor crosses a first section of the control bus and then each conductor of the control bus crosses each conductor of the local bus a plurality of times. Thus, a capacitive coupling is incurred at each cross over as discussed in the present specification with respect to the prior art figure 2. In the present claimed invention a plurality of local buses are separated from one another and have a plurality of conductors coupled in a local, clustering bus arrangement. This configuration minimizes the number of crossovers in order to reduces dynamic power dissipation, improve yield and reduce crosstalk among the brightness information carrying-conductors. Shinya is concerned with reducing the number of DAC's and thereby reducing the size of the display device as opposed to the present claimed invention which is concerned with improving the yield and reducing crosstalk among the conductors.

Accordingly, it is respectfully submitted that the present claimed invention is not anticipated by Shinya and that the rejection of Claim 1 under 35 U.S.C. § 102(b) is satisfied. Additionally, because Claims 2-6 depend from the independent Claim 1, dependent claims 2-6 also satisfy this rejection for the same reason as Claim 1. In view of the above remarks it is respectfully submitted this rejection of claims 1-6 be withdrawn.

Rejection of Claim 7-9 under 35 U.S.C. § 102(b)

Claims 7-9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Inoue et al., U.S. Patent No. 5,113,181.

The present invention as claimed in claim 7 recites a signal demultiplexer for a display panel. The signal demultiplexer includes a plurality of switch groups, each switch

group having ordinally numbered switches 1 thru n arranged sequentially. Each switch has a respective input, output and control terminals with the control terminals of all switches in each group connected to a common control terminal, and respective output terminals coupled to successive data lines on the display panel. A plurality of groups of data buses are also provided. Each group of data buses having ordinally numbered conductors 1 thru n. The ordinally numbered conductors of respective groups of data buses are coupled to input terminals of corresponding ordinally numbered switches of certain switch groups within said plurality of switch groups. A control bus includes a plurality of conductorsand is arranged to cross the plurality of groups of data buses. Connections exist between ones of the plurality of conductors of the control bus and respective common control terminals within each of said plurality of switch groups.

Inoue et al. describes a display apparatus comprising a plurality of pixels arranged in pluralities of rows and columns. This apparatus includes an N X M active matrix liquid crystal display unit having N X M pixels, each pixel being provided with a switching element. Image signal lines supply latched image signals to the switching elements and switching lines switch the switching elements. The image signal lines are divided into n blocks each having m lines which are commonly connected to one signal line through a corresponding switching element. The n lines are selectively supplied an image signal through the switching element by the image signal line, the image signal being stored in a capacitor.

Inoue et al. neither disclose nor suggest a plurality of groups of data buses, each group having ordinally numbered conductors as in the present claimed invention. Inoue et al. disclose only a plurality of conductors. Inoue et al. also neither disclose nor suggest "the ordinally numbered conductors of respective groups of data buses being coupled to input terminals of corresponding ordinally numbered switches of a certain switch groups within said plurality of switch groups" as in the present claimed invention. Inoue et al. disclose each image signal line being coupled to an input terminal of a switch in every switch

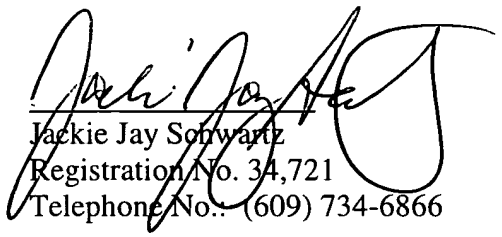
group. Furthermore, Inoue et al. neither disclose nor suggest a control bus including a plurality of conductors, said control bus arranged to cross said plurality of groups of data buses as in the present claimed invention. Inoue et al. includes a plurality of conductive lines and a plurality of switching signal lines. Each switching signal line crosses each of said plurality of conductive lines. As explained above the present claimed invention reduces dynamic power dissipation and improve yield by reducing the number of times conductors DWC(i) cross the bus of conductors DW(i). Inoue et al. is concerned with reducing the number of signal lines to reduce cost, simplify production and minimize delay of polarity. Inoue et al. is not concerned with reducing dynamic power dissipation and improve yield by reducing the number of times the conductors DWC (i) cross the bus of conductors DW (i) as in the present claimed invention. In fact, the arrangement of Inoue et al., which uses a plurality of conductive lines and a plurality of switching signal lines, increases the number of crossovers and thereby increases the capacitive coupling between the conductors. As reducing dynamic power dissipation and improve yield by reducing the number of times the local buses cross the control bus as in the present claimed invention is not a concern of Inoue et al. Inoue et al. neither discloses nor suggests such an embodiment in which a plurality of groups of data buses are crossed by the control bus as in the present claimed invention. Inoue et al. neither discloses use of a data bus or control bus but only discloses a plurality of individual conductive lines. Such limitations are included in both independent claims 7 and 8. Claim 9 is dependent on claim 8 and thus includes the limitations thereof.

Accordingly, it is respectfully submitted that the rejection of independent Claim 7 under 35 U.S.C. § 102(b) is satisfied. Claims 8 and 9 have been cancelled by this response and thus I is respectfully submitted that the rejection of these claims is now moot. Withdrawal of the rejection is thus respectfully requested.

No fee is believed due with this amendment. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

In view of all of the foregoing, it is submitted that the amended application is now in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
Roger Green Stewart



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